In The Claims:

1. (Currently Amended) An apparatus for implementing a multi-level system model, comprising:

a picokernel configured to schedule and execute one or more selected processes in an electronic device, said one or more selected processes including an isochronous process and a plesiochronous process; and

a processor coupled to said electronic device for controlling said picokernel.

2. (Original) The apparatus of claim 1, wherein said electronic device is coupled to an electronic network that is implemented according to an IEEE 1394 serial bus standard.

3. (Original) The apparatus of claim 1 wherein said electronic device is one of a consumer-electronics device, an audio-visual device, and a computer device.

4. (Original) The apparatus of claim 1 wherein said one or more selected processes include at least one of transporting time-sensitive data and processing time-sensitive data

5. (Cancelled).

6. (Currently Amended) The apparatus of ~~claim 5~~ claim 1 wherein said at least one of said isochronous process and said plesiochronous process are executed in a manner that is synchronized with isochronous cycles that are each synchronized to an isochronous clock.

7. (Currently Amended) The apparatus of claim 6 wherein said picokernel is repeatedly triggered to schedule and execute said at least ~~one of an~~ one of said isochronous process ~~and a~~ and said plesiochronous process by a cycle start signal in a manner that is synchronized with said isochronous cycles.

8. (Original) The apparatus of claim 1 wherein said picokernel includes an isochronous scheduler and a plesiochronous scheduler, said picokernel responsively invoking said isochronous scheduler in response to an isochronous cycle start signal to thereby select, schedule, and execute active isochronous processes on said electronic device, said active isochronous processes selectively generating flags to designate active plesiochronous processes, said plesiochronous scheduler then selecting, scheduling, and executing said active plesiochronous processes when all of said active isochronous processes have been executed.

9. (Original) The apparatus of claim 1 wherein said picokernel is stored in a memory device that also includes at least one of device software, a cantaloupe manager, one or more cantaloupes, one or more endochronous application program interfaces, one or more isochronous process representations, and one or more plesiochronous process representations.

10. (Original) The apparatus of claim 9 wherein said picokernel includes at least one of an isochronous scheduler, an isochronous process list, a plesiochronous scheduler, and a plesiochronous process list.

11. (Original) The apparatus of claim 9 wherein said one or more cantaloupes each includes one or more device resource identifiers that are each associated with a corresponding device resource usage value.

12. (Original) The apparatus of claim 9 wherein said one or more endochronous application program interfaces include at least one of means for installing isochronous services, means for creating and controlling endochronous processes, and means for communicating through a signaling mechanism.

13. (Original) The apparatus of claim 9 wherein said one or more isochronous process representations and said one or more plesiochronous process representations each includes one or more data structures that correspond to a respective process that has been instantiated on said electronic device, said data structures including optimized information for deterministically executing said respective process.

14. (Original) The apparatus of claim 1 wherein device software performs an initial identification procedure that includes receiving notification information for a transfer or a processing of isochronous data.

15. (Currently Amended) The apparatus of claim 1 wherein device software generates a request to one or more endochronous application program interfaces for instantiating ~~an isochronous~~ said isochronous process.

16. (Original) The apparatus of claim 15 wherein a cantaloupe manager analyzes one or more resource characterizations to determine whether sufficient device resources are available for authorizing said one or more endochronous application program interfaces to instantiate said isochronous process on said electronic device.

17. (Original) The apparatus of claim 16 wherein said one or more endochronous application program interfaces instantiate said isochronous process on said electronic device when said sufficient device resources are available on said electronic device.

18. (Original) The apparatus of claim 17 wherein said picokernel adds an isochronous process identifier to an isochronous process list when said isochronous process has been instantiated and is active on said electronic device.

19. (Original) The apparatus of claim 1 wherein said picokernel detects a cycle start signal from an isochronous clock to signify the start of an isochronous cycle.

20. (Original) The apparatus of claim 19 wherein said picokernel determines whether one or more active isochronous processes are ready to be executed on said electronic device by referencing an isochronous process list.

21. (Original) The apparatus of claim 20 wherein said picokernel invokes an isochronous scheduler when said one or more active isochronous processes are ready to be executed, and wherein said picokernel invokes a plesiochronous scheduler when said one or more active isochronous processes are not ready to be executed.

22. (Original) The apparatus of claim 21 wherein said isochronous scheduler performs a selection procedure on said one or more active isochronous processes to produce a selected isochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said isochronous process

23. (Original) The apparatus of claim 22 wherein said isochronous scheduler schedules and executes said selected isochronous process on said electronic device.

24. (Currently Amended) ~~The apparatus of claim 23 wherein~~ An apparatus for implementing a multi-level system model, comprising:

a picokernel configured to schedule and execute one or more selected processes in an electronic device, said picokernel detecting a cycle start signal from an isochronous clock to signify a start of an isochronous cycle, said picokernel determining whether one or more active isochronous processes are ready to be executed on said electronic device by referencing an isochronous process list, said picokernel invoking an isochronous scheduler when said one or more active isochronous processes are ready to be executed, said picokernel invoking a plesiochronous scheduler when said one or more active isochronous processes are not ready to be executed, said isochronous scheduler performing a selection procedure on said one or more active isochronous processes to produce a selected isochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said isochronous process, said isochronous scheduler scheduling and executing said selected isochronous process on said electronic device, said selected isochronous process ~~sets a~~ setting a plesiochronous flag to thereby designate an active plesiochronous process for scheduling and execution on said electronic device, said active isochronous process notifying said picokernel which responsively adds a corresponding plesiochronous process identifier to a plesiochronous process list; and

a processor coupled to said electronic device for controlling said picokernel.

25. (Original) The apparatus of claim 23 wherein said picokernel sequentially selects, schedules, and executes a series of isochronous processes using said isochronous scheduler.

26. (Original) The apparatus of claim 1 wherein said picokernel waits until all isochronous processes for a current isochronous cycle have been executed, said picokernel then determining whether one or more active flagged plesiochronous processes are ready to be executed on said electronic device by referencing a plesiochronous process list.

27. (Original) The apparatus of claim 26 wherein said picokernel invokes a plesiochronous scheduler when said one or more active flagged plesiochronous processes are ready to be executed, and wherein said picokernel waits for a new cycle start signal when said one or more active flagged plesiochronous processes are not ready to be executed.

28. (Original) The apparatus of claim 27 wherein said plesiochronous scheduler performs a selection procedure on said one or more active flagged plesiochronous processes to produce a selected plesiochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said plesiochronous process, said plesiochronous scheduler then scheduling and executing said selected plesiochronous process on said electronic device.

29. (Currently Amended) ~~The apparatus of claim 28 wherein~~ An apparatus for implementing a multi-level system model, comprising:

a picokernel configured to schedule and execute one or more selected processes in an electronic device, said picokernel waiting until all isochronous processes for a current isochronous cycle have been executed, said picokernel then determining whether one or more active flagged plesiochronous processes are ready to be executed on said electronic device by referencing a plesiochronous process list, said picokernel invoking a plesiochronous scheduler when said one or more active flagged plesiochronous processes are ready to be executed, said picokernel waiting for a new cycle start signal when said one or more active flagged plesiochronous processes are not ready to be executed, said plesiochronous scheduler performing a selection procedure on said one or more active flagged plesiochronous processes to produce a selected plesiochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said plesiochronous process, said plesiochronous scheduler then scheduling and executing said selected plesiochronous process on said electronic device, said picokernel ~~halts~~ halting said plesiochronous process and ~~marks~~ marking said plesiochronous process for a subsequent completion in response to an interrupt event, said interrupt event including one of a cycle start signal and an exochronous interrupt, said picokernel beginning a new isochronous cycle in response to said cycle start signal, said picokernel switching to an exochronous processing for executing required system tasks in response to said exochronous interrupt; and

a processor coupled to said electronic device for controlling said picokernel.

30. (Original) The apparatus of claim 28 wherein said picokernel sequentially selects, schedules, and executes a series of plesiochronous processes using said plesiochronous scheduler, said picokernel returning to wait for said new cycle start signal when all of said series of plesiochronous processes have been executed.

31. (Currently Amended) A method for implementing a multi-level system model, comprising the steps of:

scheduling one or more selected processes in an electronic device by using a picokernel, said one or more selected processes including an isochronous process and a plesiochronous process;

executing said one or more selected processes by using said picokernel; and

controlling said picokernel by using a processor.

32. (Original) The method of claim 31, wherein said electronic device is coupled to an electronic network that is implemented according to an IEEE 1394 serial bus standard.

33. (Original) The method of claim 31 wherein said electronic device is one of a consumer-electronics device, an audio-visual device, and a computer device.

34. (Original) The method of claim 31 wherein said one or more selected processes include at least one of transporting time-sensitive data and processing time-sensitive data

35. (Cancelled).

36. (Currently Amended) The method of ~~claim 35~~ claim 31 wherein said at least one of said isochronous process and said plesiochronous process are executed in a manner that is synchronized with isochronous cycles that are each synchronized to an isochronous clock.

37. (Currently Amended) The method of claim 36 wherein said picokernel is repeatedly triggered to schedule and execute said at least ~~one of an~~ one of said isochronous process ~~and a~~ and said plesiochronous process by a cycle start signal in a manner that is synchronized to said isochronous cycles.

38. (Original) The method of claim 31 wherein said picokernel includes an isochronous scheduler and a plesiochronous scheduler, said picokernel responsively invoking said isochronous scheduler in response to an isochronous cycle start signal to thereby select, schedule, and execute active isochronous processes on said electronic device, said active isochronous processes selectively generating flags to designate active plesiochronous processes, said plesiochronous scheduler then selecting, scheduling, and executing said active plesiochronous processes when all of said active isochronous processes have been executed.

39. (Original) The method of claim 31 wherein said picokernel is stored in a memory device that also includes at least one of device software, a cantaloupe manager, one or more cantaloupes, one or more endochronous application program interfaces, one or more isochronous process representations, and one or more plesiochronous process representations.

40. (Original) The method of claim 39 wherein said picokernel includes at least one of an isochronous scheduler, an isochronous process list, a plesiochronous scheduler, and a plesiochronous process list.

41. (Original) The method of claim 39 wherein said one or more cantaloupes each includes one or more device resource identifiers that are each associated with a corresponding device resource usage value.

42. (Original) The method of claim 39 wherein said one or more endochronous application program interfaces include at least one of means for installing isochronous services, means for creating and controlling endochronous processes, and means for communicating through a signaling mechanism.

43. (Original) The method of claim 39 wherein said one or more isochronous process representations and said one or more plesiochronous process representations each includes one or more data structures that correspond to a respective process that has been instantiated on said electronic device, said data structures including optimized information for deterministically executing said respective process.

44. (Original) The method of claim 31 wherein device software performs an initial identification procedure that includes receiving notification information for a transfer or a processing of isochronous data.

45. (Currently Amended) The method of claim 31 wherein device software generates a request to one or more endochronous application program interfaces for instantiating ~~an isochronous~~ said isochronous process.

46. (Original) The method of claim 45 wherein a cantaloupe manager analyzes one or more resource characterizations to determine whether sufficient device resources are available for authorizing said one or more endochronous application program interfaces to instantiate said isochronous process on said electronic device.

47. (Original) The method of claim 46 wherein said one or more endochronous application program interfaces instantiate said isochronous process on said electronic device when said sufficient device resources are available on said electronic device.

48. (Original) The method of claim 47 wherein said picokernel adds an isochronous process identifier to an isochronous process list when said isochronous process has been instantiated and is active on said electronic device.

49. (Original) The method of claim 31 wherein said picokernel detects a cycle start signal from an isochronous clock to signify the start of an isochronous cycle.

50. (Original) The method of claim 49 wherein said picokernel determines whether one or more active isochronous processes are ready to be executed on said electronic device by referencing an isochronous process list.

51. (Original) The method of claim 50 wherein said picokernel invokes an isochronous scheduler when said one or more active isochronous processes are ready to be executed, and wherein said picokernel invokes a plesiochronous scheduler when said one or more active isochronous processes are not ready to be executed.

52. (Original) The method of claim 51 wherein said isochronous scheduler performs a selection procedure on said one or more active isochronous processes to produce a selected isochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said isochronous process

53. (Original) The method of claim 52 wherein said isochronous scheduler schedules and executes said selected isochronous process on said electronic device.

54. (Currently Amended) ~~The method of claim 53 wherein~~ A method for implementing a multi-level system model, comprising the steps of:

scheduling one or more selected processes in an electronic device by using a picokernel, said picokernel detecting a cycle start signal from an isochronous clock to signify a start of an isochronous cycle, said picokernel determining whether one or more active isochronous processes are ready to be executed on said electronic device by referencing an isochronous process list, said picokernel invoking an isochronous scheduler when said one or more active isochronous processes are ready to be executed, said picokernel invoking a plesiochronous scheduler when said one or more active isochronous processes are not ready to be executed, said isochronous scheduler performing a selection procedure on said one or more active isochronous processes to produce a selected isochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said isochronous process, said isochronous scheduler scheduling said selected isochronous process on said electronic device, said selected isochronous process ~~sets a~~ setting a plesiochronous flag to thereby designate an active plesiochronous process for scheduling and execution on said electronic device, said active isochronous process notifying said picokernel which responsively adds a corresponding plesiochronous process identifier to a plesiochronous process list;

executing said one or more selected processes by using said picokernel; and

controlling said picokernel by using a processor.

55. (Original) The method of claim 53 wherein said picokernel sequentially selects, schedules, and executes a series of isochronous processes using said isochronous scheduler.

56. (Original) The method of claim 31 wherein said picokernel waits until all isochronous processes for a current isochronous cycle have been executed, said picokernel then determining whether one or more active flagged plesiochronous processes are ready to be executed on said electronic device by referencing a plesiochronous process list.

57. (Original) The method of claim 56 wherein said picokernel invokes a plesiochronous scheduler when said one or more active flagged plesiochronous processes are ready to be executed, and wherein said picokernel waits for a new cycle start signal when said one or more active flagged plesiochronous processes are not ready to be executed.

58. (Original) The method of claim 57 wherein said plesiochronous scheduler performs a selection procedure on said one or more active flagged plesiochronous processes to produce a selected plesiochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said plesiochronous process, said plesiochronous scheduler then scheduling and executing said selected plesiochronous process on said electronic device.

59. (Currently Amended) ~~The method of claim 58 wherein~~ A method for implementing a multi-level system model, comprising the steps of:

scheduling one or more selected processes in an electronic device by using a picokernel, said picokernel waiting until all isochronous processes for a current isochronous cycle have been executed, said picokernel then determining whether one or more active flagged plesiochronous processes are ready to be executed on said electronic device by referencing a plesiochronous process list, said picokernel invoking a plesiochronous scheduler when said one or more active flagged plesiochronous processes are ready to be executed, said picokernel waiting for a new cycle start signal when said one or more active flagged plesiochronous processes are not ready to be executed, said plesiochronous scheduler performing a selection procedure on said one or more active flagged plesiochronous processes to produce a selected plesiochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said plesiochronous process, said plesiochronous scheduler then scheduling said selected plesiochronous process on said electronic device;

executing said one or more selected processes by using said picokernel, said picokernel ~~halts~~ halting said plesiochronous process and ~~marks~~ marking said plesiochronous process for a subsequent completion in response to an interrupt event, said interrupt event including one of a cycle start signal and an exochronous interrupt, said picokernel beginning a new isochronous cycle in response to said cycle start signal, said picokernel switching to an exochronous processing for executing required system tasks in response to said exochronous interrupt; and

controlling said picokernel by using a processor.

60. (Original) The method of claim 58 wherein said picokernel sequentially selects, schedules, and executes a series of plesiochronous processes using said plesiochronous scheduler, said picokernel returning to wait for said new cycle start signal when all of said series of plesiochronous processes have been executed.

61. (Original) A computer-readable medium comprising program instructions for implementing a multi-level system model by performing the steps of:

scheduling one or more selected processes in an electronic device by using a picokernel;

executing said one or more selected processes by using said picokernel; and

controlling said picokernel by using a processor.

62. (Original) An apparatus for implementing a multi-level system model, comprising:

means for scheduling one or more selected processes in an electronic device;

means for executing said one or more selected processes; and

means for controlling said means for scheduling and said means for executing.